

What is Claimed is:

1 1. In a target processor, an apparatus for
2 controlling the response to an event, the apparatus
3 comprising:

4 a central processing unit;

5 first signal paths from selected apparatus in the
6 central processing unit, the selected apparatus receiving
7 predetermined event signals;

8 second signal paths from target processor mode
9 identifying the mode of operation a central of the of
10 operation signals

11 a unit coupled to the first and second signal paths,
12 the unit providing a response to event signals the signals
13 on the second signal paths.

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15 2. The apparatus as recited in claim 1 wherein the
16 unit receives control signals from a user.

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18 3. The apparatus as recited in claim 1 wherein the
19 response to an event signal detected during a first mode of
20 instruction code execution is delayed until a second mode
21 of instruction code execution.

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23 4. The apparatus as recited in claim 3 wherein the
24 first mode of instruction code execution a background mode
25 of instruction execution and a second mode of instruction

1 execution was a foreground or program mode of instruction
2 execution.

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4 5. The apparatus as recited in claim 1 wherein the
5 unit is a trigger unit and wherein the response to an event
6 signal is the generation of a trigger signal.

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8 6. The apparatus as recited in claim 5 further
9 comprising trace stream generation apparatus, wherein the
10 trigger unit generates a sync signal in response to a
11 trigger signal.

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13 7. The method of responding to an event detected in
14 a target processor, the method comprising:

15 providing an immediate response to an event detected
16 during a first mode of instruction execution; and

17 providing a delayed response to an event detected
18 during a second mode of instruction execution, the response
19 to the event delayed until the target processor enters a
20 second mode of instruction execution.

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22 8. The method as recited in claim 7 wherein the
23 first mode of instruction execution is a background or
24 program code execution mode and the second mode of
25 instruction execution is a foreground ground or interrupt
26 service routine program code execution mode.

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1 9. The method as recited in claim 8 further
2 comprising:

3 in response to first control signals, providing an
4 immediate response to an event during the first and the
5 second mode of code execution.

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7 10. The method as recited in claim 7 wherein the
8 immediate and the delayed response is the generation of a
9 trigger signal.

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11 11. A test and debug system in a target processor,
12 the system comprising:

13 a central processing unit, the central processing unit
14 generating event signals and mode of operation signals; and

15 a logic unit responsive to the event signals and to
16 the mode of operation signals, the logic unit providing an
17 immediate response to an event signal in a first mode of
18 operation, the logic unit providing a response to an event
19 signal during second mode of operation in the first mode of
20 operation.

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22 12. The system as recited in claim 11 wherein the
23 first mode of operation is a background or program mode of
24 instruction execution and the second mode of operation is a
25 background or interrupt service routine mode of instruction
26 execution.

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1 13. The system as recited in claim 11 wherein the
2 response is a generation of trigger signal.

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4 14. The system as recited in claim 11 wherein, in
5 response to first control signals, the response of the
6 logic unit to an event is generated immediately in both the
7 first and the second mode of operation.

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9 15. The system as recited in claim 14 further
10 comprising trace stream generating apparatus, the response
11 of the logic unit is the generation of a trigger signal,
12 the trigger signal resulting in a sync marker in the trace
13 stream.

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